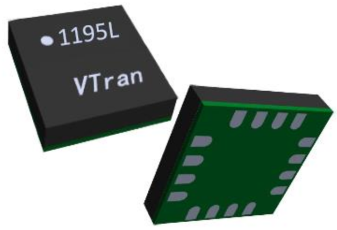
1. Product Overview

The VCM1195L is a three-axis magnetic sensor with very low power consumption developed specifically for IoT applications. This surface-mount, small sized chip has integrated magnetic sensors with signal condition ASIC, it offers the advantages of low noise, high accuracy, low power consumption, offset cancellation and temperature compensations.



The VCM1195L is based on Anisotropic Magneto-Resistive (AMR) and CMOS technology. Linear three axis magnetic sensor along with custom-designed 18-bit ADC and power management ASIC, it provides digital signal with I²C serial bus.

The VCM1195L is in a 3x3x0.9mm^3 surface mount 16-pin land grid array (LGA) package. Applications for the VCM1195L include vehicle detection for parking space, smart door lock, and other battery supplied IoT devices.

2. Key Features

Features	Benefits
Three-Axis Magneto-Resistive Sensors in a 3x3x0.9 mm^3 Land Grid Array Package (LGA), Guaranteed to Operate Over an Temperature Range of -40°C to +85°C.	Small Size for Highly Integrated Products. Signals Have Been Digitized And Calibrated
18 Bit ADC With Low Noise AMR Sensors Achieves 1 Milli-Gauss Field Resolution	Enables <1 degree Earth Magnetic Field Angle Changes. Allows for Small Field Detections
Wide Magnetic Field Range (±8 Gauss)	Maximizes Sensor's Full Dynamic Range and Resolution
Temperature Compensated Data Output and Temperature Output	Automatically Maintains Sensor's Sensitivity Under Wide Operating Temperature Range
I2C (Standard ,Fast Modes) Interface	Simplified Digital Outputs
Low Operation Voltage (2.16V To 3.6V) and Low Power Consumption (Standby Current 3μA)	Compatible with Battery Powered Applications
Lead Free Package Construction	RoHS Compliance
Software And Algorithm Support Available	Compassing Heading, Hard Iron, Soft Iron, and Auto Calibration Libraries Available

3. Applications

Static Vehicle Detection	Typical Applications Include Geomagnetic Parking Detector, Parking Lock, etc
Consumer Electronics	Typical Applications Include Door Lock Position Detection, Sweeper Direction Control, Notebooks Power Control, etc
Navigation	Typical Applications Include Auto Navigation Systems, and Personal Navigation Devices etc

4. Module/Circuit Diagram

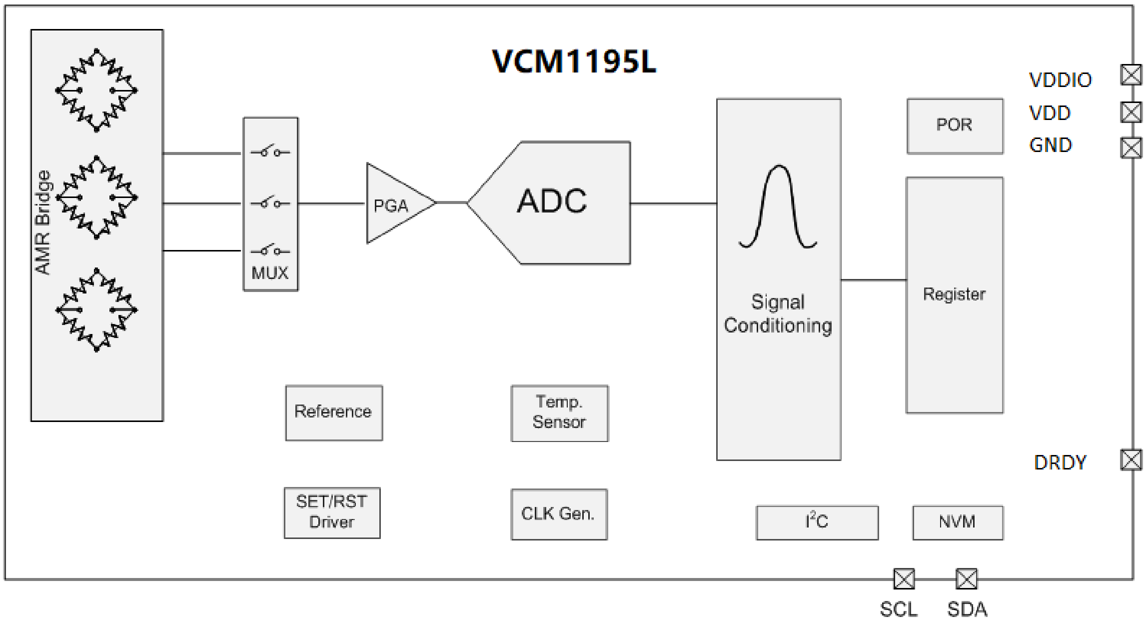


Figure 1 Block Diagram

Table 1 Block Function

Block	Function
AMR Bridge	3 axis magnetic sensors
MUX	Multiplexer for sensor channels
PGA	Programmable gain amplifier for sensor signals
ADC	18 bit Analog-to-Digital converter
Signal Conditioning	Digital blocks for magnetic signal calibration and compensation
I^2C	Interface logic data I/O
NVM	Non-Volatile memory for calibrated parameters
SET/RST Driver	Internal driver to initialize magnetic sensor
Reference	Voltage/Current reference for internal biasing
Clock Gen.	Internal oscillator for internal operation
POR	Power on reset
Temperature Sensor	Temperature sensor for internal sensitivity/offset compensation, and temperature output

5. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Tested at 25°C except stated otherwise.)

Parameter	MIN.	MAX.	Units
VDDIO	-0.3	5.4	V
VDD	-0.3	5.4	V
Storage Temperature	-40	125	°C
Exposed to Magnetic Field (all directions)		50000	Gauss
Reflow Classification	MSL 3, 260°C Peak Temperature		

6. Electrical Performance

Table 3 Specifications (* Tested and specified at 25°C except stated otherwise.)

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDD	2.16		3.6	V
I/O Voltage	VDDIO	1.65		3.6	V
Standby Current	Total Current on VDD and VDDIO		3		μA
Supply Current [1]	Measurement Frequency = 1Hz		5.5		μA
Sensor Field Range	Full Scale	-8		+8	Gauss
Sensitivity [2]	Field Range = ±8G		11000		LSB/G
Linearity (Best fit linear curve)	Field Range = ±2G		0.05		%FS
Hysteresis	All Ranges		0.1		%FS
Cross Axis Sensitivity	Cross field = 1 Gauss, Happlied = ±2 Gauss		0.05		%/G
Offset			±10		mG
Sensitivity Tempco	Ta = -40℃~85℃		±0.05		%/℃
Temperature Sensor Sensitivity	Ta = -40℃~85℃		14		LSB/℃
Digital Resolution	Change with Gain	0.1		1.0	mGauss
Field Resolution	Standard deviation 100 Data, FS ±2G		1.2		mGauss
X-Y-Z Orthogonality	Sensitivity Directions		90±1		Degree
Operating Temperature		-40		85	℃
ESD	HB Model	2000			V
	Charge Device Model	750			

Note : [1] The operating current is related to measuring frequency.

Calculation formula(uA): $2.5 \times frequency + 3$

Note :[2] Sensitivity is calibrated at zero field, it is slightly decreased at high fields.

7. I/O Characteristics

Table 4 I/O Characteristics

Parameter	Symbol	Pin	Condition	Min.	TYP.	Max.	Unit
Voltage Input High Level 1	$V_{IH}1$	SDA, SCL		0.7*VDDIO		VDDIO+0.3	V
Voltage Input Low Level 1	$V_{IL}1$	SDA, SCL		-0.3		0.3*VDDIO	V
Voltage Output High Level	V_{OH}	INT	Output Current ≥-100uA	0.8*VDDIO			V
Voltage Output Low Level	V_{OL}	INT, SDA	Output Current ≤100uA(INT) Output Current ≤1mA (SDA)			0.2*VDDIO	V

8 Package Pin Configurations

8.1 Package 3-D View

Arrow indicates direction of magnetic field that generates a negative output reading in normal measurement configuration.

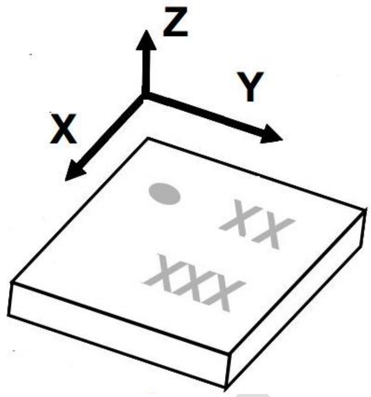


Figure 2 Package 3-D View

Table 5 Pin Configurations

PIN No.	PIN NAME	Function
1	SCL	Serial Clock – I^2C Master/Slave Clock
2	VDD	Power Supply (2.16V to 3.6V)
3	NC	Not to be Connected
4	VDD	Power Supply
5	NC	Not to be Connected
6	NC	Not to be Connected
7	NC	Not to be Connected
8	SETP	Set/Reset Strap Positive – S/R Capacitor (C2) Connection
9	GND	Supply Ground
10	C1	Reservoir Capacitor (C1) Connection
11	GND	Supply Ground
12	SETC	S/R Capacitor (C2) Connection – Driver Side
13	VDDIO	IO Power Supply (1.71V to VDD)
14	NC	Not to be Connected
15	NC	Not to be Connected
16	SDA	Serial Data – I^2C Master/Slave Data

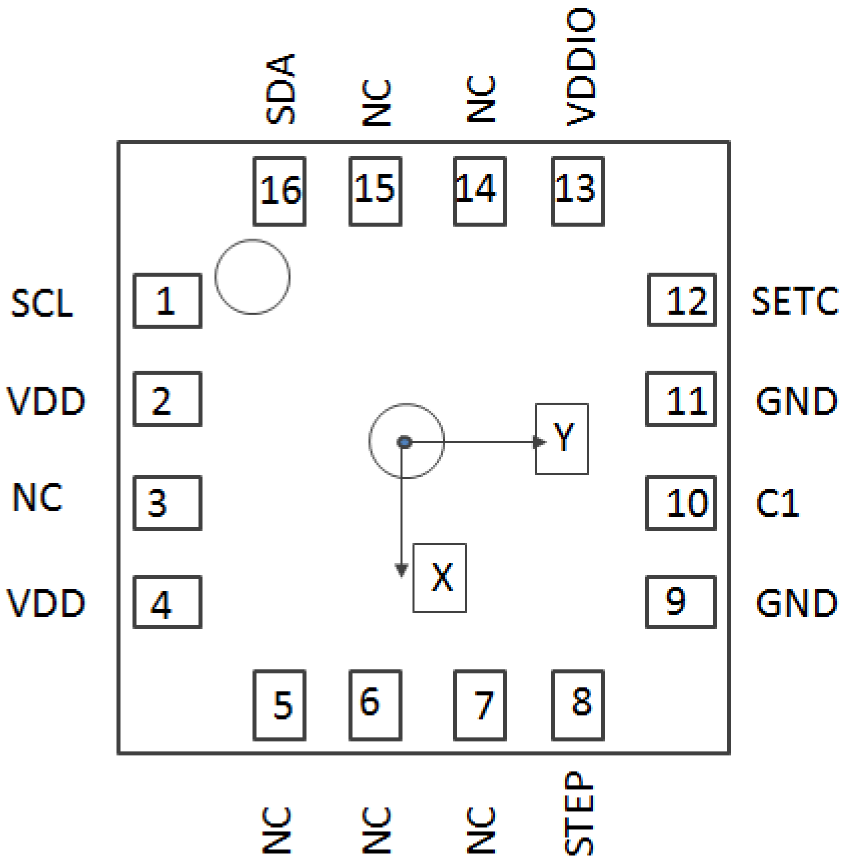


Figure 3 TOP VIEW (looking through)

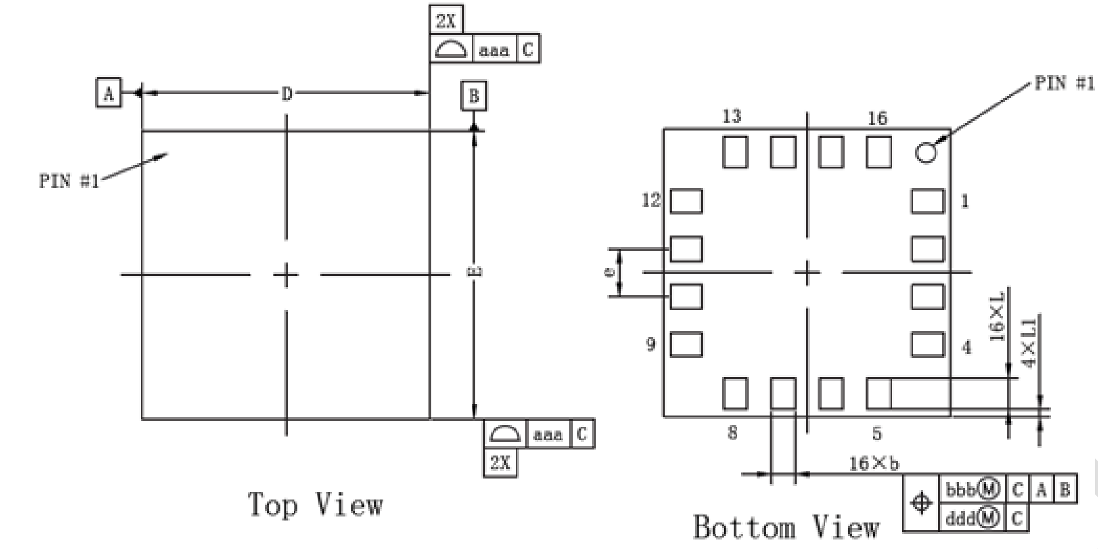
8.2 Package Outlines

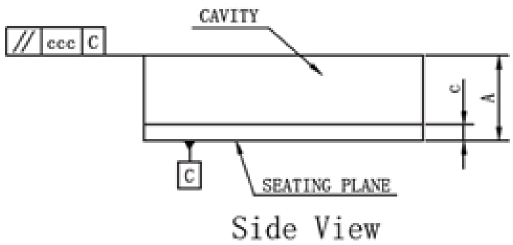
8.2.1 Package Type

LGA (Land Grid Array)

8.2.2 Package Size

3mm (Length)*3mm (Width)*0.9mm (Height)





symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.820	0.920	1.020	0.032	0.036	0.040
c	0.130	0.170	0.210	0.005	0.007	0.008
D	2.900	3.000	3.100	0.114	0.118	0.122
E	2.900	3.000	3.100	0.114	0.118	0.122
L	0.250	0.325	0.400	0.010	0.013	0.016
L1	0.000	0.075	0.150	0.000	0.003	0.006
e	—	0.500	—	—	0.020	—
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa		0.100			0.004	
bbb		0.150			0.006	
ccc		0.100			0.004	
ddd		0.080			0.003	
eee		0.150			0.006	

Figure 4 Package Size

8.2.3 Marking

Tracking code:

Text1: D-Fixed code, X-Product Type

Text2: Product Batch Number

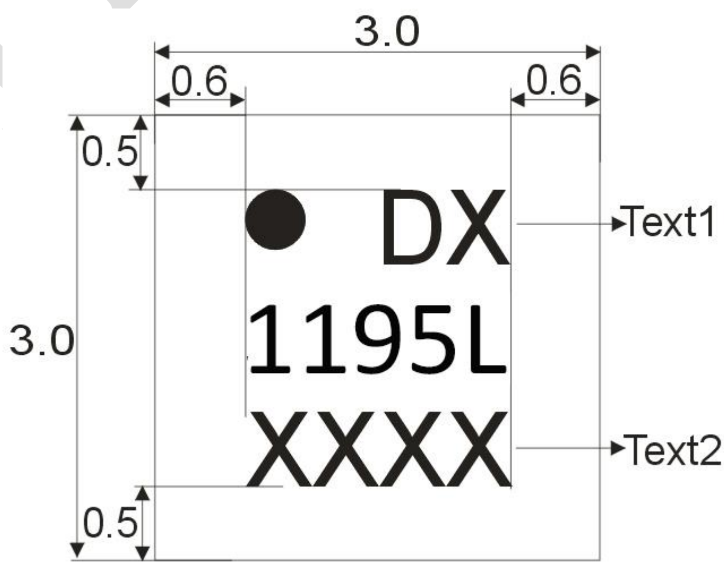


Figure 5 Chip Marking

9. External Connection

9.1 Single Supply connection

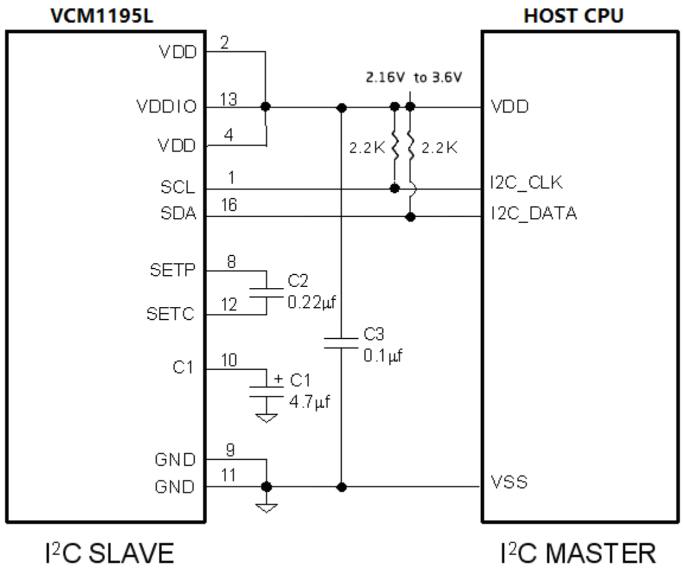


Figure6 Single Supply Connection

9.2 Mounting Considerations

The following is the recommend printed circuit board (PCB) footprint for the VCM1195L. Due to the fine pitch of the pads, the footprint should be properly centered in the PCB.

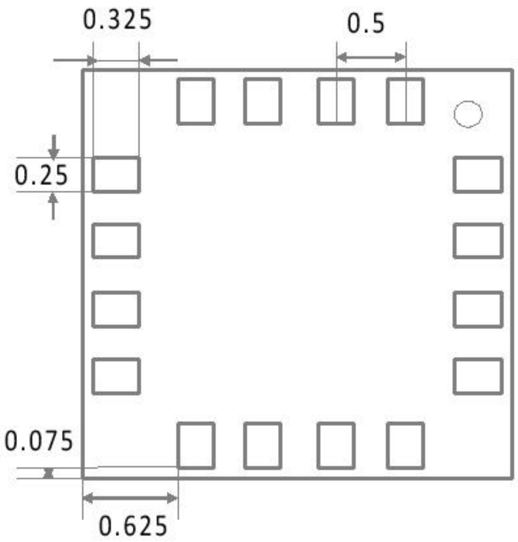


Figure 7 VCM1195L PCB footprint

9.3 Layout Considerations

Besides keeping all components that may contain ferrous materials (nickel, etc.) away from the sensor on both sides of the PCB, it is also recommended that there is no conducting copper line under/near the sensor in any of the PCB layers.

9.3.1 Solder Paste

A 4 mil stencil and 100% paste coverage is recommended for the electrical contact pads.

9.3.2 Reflow Assembly

This device is classified as MSL 3 with 260°C peak reflow temperature. As specified by JEDEC, parts with an MSL 3 rating require baking prior to soldering, if the part is not kept in a continuously dry (< 10% RH) environment before assembly. Reference IPC/JEDEC standard J-STD-033 for additional information.

No special reflow profile is required for VCM1195L, which is compatible with lead eutectic and lead-free solder paste reflow profiles. VTRAN recommends adopting solder paste manufacturer's guidelines. Hand soldering is not recommended.

9.3.3 External Capacitors

The external capacitors C1 should be ceramic type with low ESR characteristics. The exact ESR value is not critical, but values less than 200 milli-ohms are recommended. Reservoir capacitor C1 is nominally 4.7 μF in capacitance, with the set/reset capacitor C2 nominally 0.22 μF in capacitance. Low ESR characteristics may not be in many small SMT ceramic capacitors (0402), so be prepared to up-size the capacitors to gain low ESR characteristics.

10. Basic Device Operation

10.1 Anisotropic Magneto-Resistive Sensors

The VCM1195L magneto-resistive sensor circuit consists of tri-axial sensors and application specific support circuits to measure magnetic fields. With a DC power supply is applied to the sensor two terminals, the sensor converts any incident magnetic field in the sensitive axis directions to a differential voltage output. The ASIC then amplifies and processes the signal to have a digital output.

The device has an offset cancellation function to eliminate sensor and ASIC offsets. It also applies a self-aligned magnetic field to restore magnetic state before each measurement to ensure high accuracy. Because of these features, the VCM1195L doesn't need to calibrate every time in most of application situations. It may need to be calibrated once in a new system or a system changes a new battery.

10.2 Power Management

There are two power supply pins to the device. VDD provides power for all the internal analog and digital functional blocks. VDDIO provides power for digital I/O and logic. It always works with VDDIO equal to VDD, the single supply mode.

The device should turn-on both power pins in order to operate properly. When the device is powered on, all registers are reset by POR, then the device transits to the standby mode and waits for further commands.

Table 6 provides references for four power states. Transitions between power state 2 and power state 3 are prohibited, due to leakage current concerns.

Table 6 Power States

Power State	VDD	VDDIO	Power State description
1	0V	0V	Device Off, No Power Consumption
2	0V	1.65v~3.6v	Device Off, Unpredictable Leakage Current on VDD due to Floating Node.
3	2.16v~3.6v	0	Device Off, Same Current as Standby Mode
4	2.16v~3.6v	1.65v~3.6v	Device On, Enters Standby Mode after POR. In Operation Mode, Only Take 1mS Measurement, Then Enter in Standby Mode.

10.3 Power On/Off Time

Table 7 Time Required for Power On/Off

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
POR Completion Time	PORT	Time Period After VDD and VDDIO at Operating Voltage to Ready for I²C Command and Analogy Measurement.			350	μs
Power off Voltage	SDV	Voltage that Device Considers to be Power Down.			0.2	V
Power on Interval	PINT	Time Period Required for Voltage Lower Than SDV to Enable Next POR	100			μs

After the device is powered on, some time periods are required for the device fully functional. The external power supply requires a time period for voltage to ramp up (PSUP), it is typically 50 milli-second. However it isn't controlled by the device. The Power-On-Reset time period (PORT) includes time to reset all the logics, load values in NVM to proper registers, enter the standby mode and get ready for analogy measurements. The power on/off time related to the device is in Table 7.

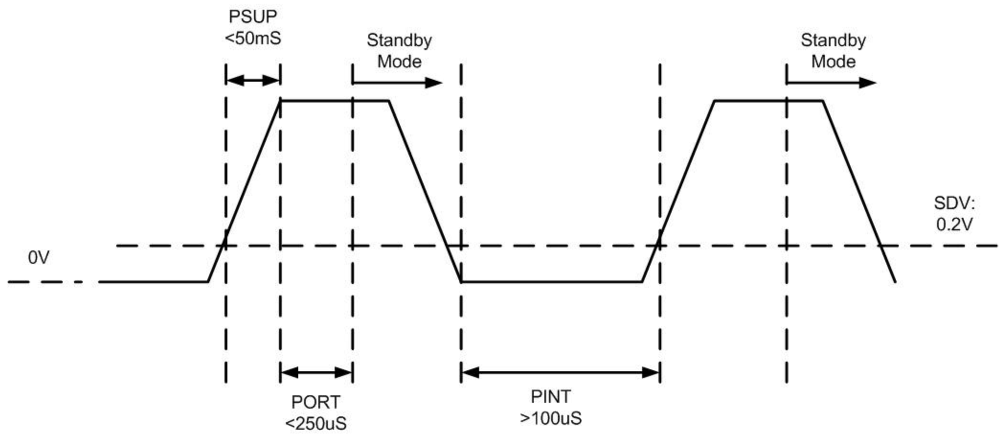


Figure 8 Power On/Off Timing

10.4 Communication Bus Interface I²C

This device will be connected to a serial interface bus as a slave device under the control of a master device, such as the processor. Control of this device is carried out via I²C.

This device is compliant with I²C-Bus Specification, document number: 9398 393 40011. As an I²C compatible device, this device has a 7-bit serial address and supports I²C protocols. This device supports standard and fast speed modes, 100kHz and 400kHz, respectively. External pull-up resistors are required to support all these modes.

10.5 Internal Clock

The device has an internal clock for internal digital logic functions and timing management. This clock is not available to external usage.

10.6 Temperature Output

VCM1195L has a built-in temperature sensor, it can provide temperature reading for other applications. The output is placed in Temperature Output Registers (07H and 08H). The temperature is calibrated for its sensitivity.

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	Bit 0
07H	T<5:0>							
08H			T<11:6>					

11. Modes Of Operation

11.1 Modes Transition

The device has two different operational modes, Standby and Measurement, controlled by register bit 'MODE'. The default mode is Standby. When MODE bit has been changed to measurement mode, the device will take a single set of measurement data send to the data registers, then it automatically enters the Standby mode, no extra mode instruction is required, however, the MODE bit need to be cleared by software.

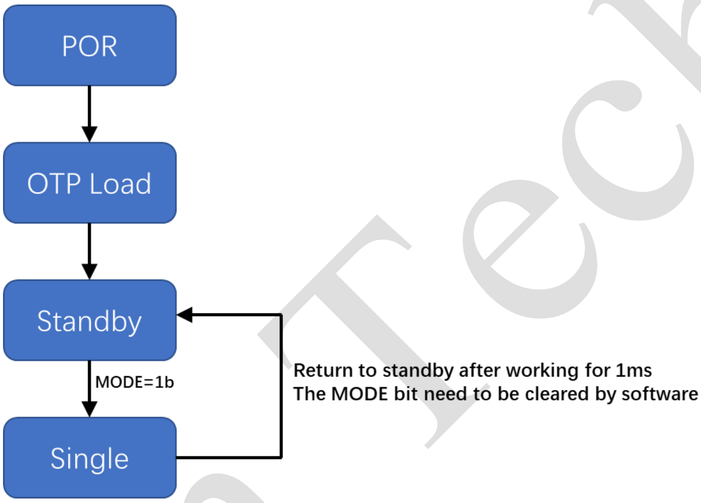


Figure 9 Operation Flow

11.2 Read Sequence

Complete magnetometer data read-out can be done as follow steps.

✧ Data protection, if any of the six data register is accessed, data protection starts. During Data protection period, data register cannot be updated until the last bits 06H have been read.

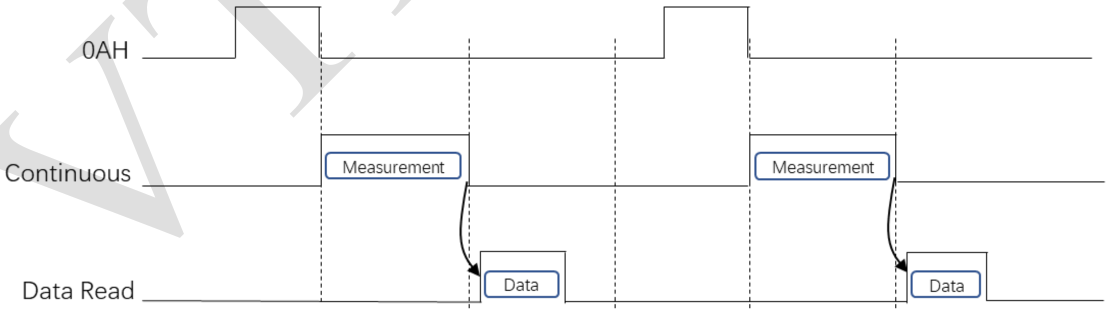


Figure 10 Single Read Sequence

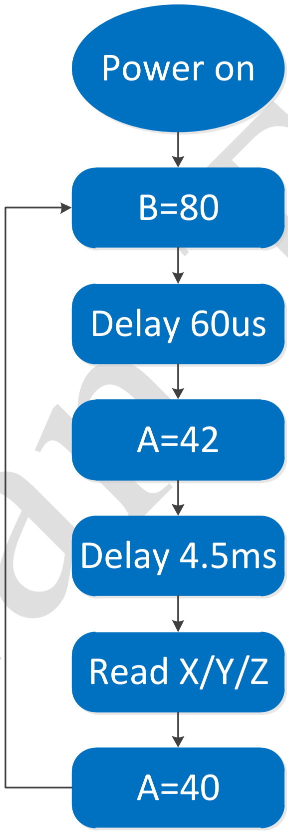
11.3 Standby Mode

Standby mode is the default state of VCM1195L upon POR and soft reset, only few function blocks are activated in this mode, which keeps power consumption as low as possible. In this state, register values are hold on by an ultra-low power LDO, I^{2}C interface can be woken up by reading or writing any registers.

There is no magnetometer measurement in the Standby mode. Internal clocking is also halted.

11.4 Measurement Mode

During measurement mode, the device makes a single measurement and places the measured data in data output registers. After the measurement is complete and output data registers are updated, the device is automatically placed in standby mode and then the operation configuration register can be allowed. Before measuring again, the Mode Register has to be changed to Standby mode by setting MODE bit (0x0AH:1b=0). Settings in any configuration register affect the measurement data, when in the measurement mode.(??) All registers maintain values while in the measurement mode. VCM1195L can share the I^2C bus with other devices on the network, and does not occupy the I^2C bus during measurement. The detailed operation method is shown in the figure below.



12. Application Examples

12.1 Measurement Example

✧ Read data register 00H ~ 06H.

12.2 Standby Example

✧ Write Register 0AH by 0x40

12.3 Measurement Example

✧ ____Write Register 0AH by 0x42

Clear mode bit 0AH by 0x40

12.4 Soft Reset Example

✧ Write Register 0BH by 0x80

12.5 Temperature Compensation

Temperature compensation needs MCU cooperation. We can provide easy to use library files of temperature compensation. Call “Compute_TEMPERATURE(hdata)” in program, return the temperature compensation X/Y/Z data.

For more information , Call our sales or download “Application note”

13 I²C Commucation Protocol

13.1 I²C Timings

Below table and graph describe the I²C communication protocol times

Table 8 I²C Timings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Clock	f_{scl}		0		400	kHz
SCL Low Period	t_{low}		1			μs
SCL High Period	t_{high}		1			μs
SDA Setup Time	t_{sudat}		0.1			μs
SDA Hold Time	t_{hddat}		0		0.9	μs
Start Hold Time	t_{hdsta}		0.6			μs
Start Setup Time	t_{susta}		0.6			μs
Stop Setup Time	t_{susto}		0.6			μs
New Transmission Time	t_{buf}		1.3			μs
Rise Time	t_r					μs
Fall Time	t_f					μs

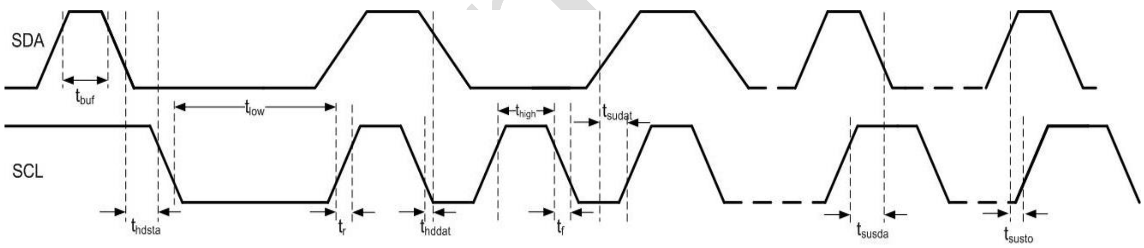


Figure 11 I²C Timing Diagram

13.2 I²C R/W Operation

13.2.1 Abbreviation

Table 9 Abbreviation

SACK	Acknowledged by slave
MACK	Acknowledged by master
NACK	Not acknowledged by master
RW	Read/Write

13.2.2 Start/Stop/ACK

START: Data transmission begins with a high to transition on SDA while SCL is held high. Once I²C transmission starts, the bus is considered busy.

STOP: STOP condition is a low to high transition on SDA line while SCL is held high.

ACK: Each byte of data transferred must be acknowledged. The transmitter must release the SDA line during the acknowledge pulse while the receiver mush then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

NACK: If the receiver doesn't pull down the SDA line during the high period of the acknowledge clock cycle, it's recognized as NACK by the transmitter.

13.2.3 I^{2}C Address

The default I^{2}C Address is OC: 0001100.
More I^{2}C Address can be obtained through factory change.

13.2.4 I^{2}C Write

I^{2}C write sequence begins with start condition generated by master followed by 7 bits slave address and a write bit (R/W=0). The slave sends an acknowledge bit (ACK=0) and releases the bus. The master sends the one byte register address. The slave again acknowledges the transmission and waits for 8 bits data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Table 10 I^{2}C Write

START	Slave Address							R W	SACK	Register Address (0x0A)								SACK	Data (0x42)								SACK	STOP
	0	0	0	1	1	0	0	0		0	0	0	0	1	0	1	0		0	1	0	0	0	0	1	0		

13.2.5 I^{2}C Read

I^{2}C write sequence consists of a one-byte I^{2}C write phase followed by the I^{2}C read phase. A start condition must be generated between two phase. The I^{2}C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (R/W=1). Then master releases the bus and waits for the data bytes to be read out from slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACK from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.

The register address is automatically incremented and more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the current I^{2}C write command.

Table 11 I²C Read

<table>
<tr><td rowspan="2">START</td><td colspan="7">Slave Address</td><td>RW</td><td rowspan="2">SACK</td><td colspan="8">Register Address (0x00)</td><td rowspan="2">SACK</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td rowspan="2">START</td><td colspan="7">Slave Address</td><td>RW</td><td rowspan="2">SACK</td><td colspan="8">Data (0x00)</td><td rowspan="2">MACK</td><td colspan="8">Data (0x01)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td rowspan="2">MACK</td><td colspan="8">Data (0x02)</td><td rowspan="2">MACK</td><td colspan="8">………………………………….</td><td rowspan="2">MACK</td><td colspan="8">Data (0x07)</td><td rowspan="2">NACK</td><td rowspan="2">STOP</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td colspan="8">………………………………….</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
</table>

14. Registers

14.1 Register Map

The table below provides a list of the 8-bit registers embedded in the device and their respective function and addresses.

Table 12 Register Map

Addr.	7	6	5	4	3	2	1	0	Access
00H	Data Output X LSB Register XOUT[9:2]								Read only
01H	Data Output X MSB Register XOUT[17:10]								Read only
02H	Data Output Y LSB Register YOUT[9:2]								Read only
03H	Data Output Y MSB Register YOUT[17:10]								Read only
04H	Data Output Z LSB Register ZOUT[9:2]								Read only
05H	Data Output Z MSB Register ZOUT[17:10]								Read only
06H			Data Output Z LSB <1:0>		Data Output Y LSB <1:0>		Data Output X LSB <1:0>		Read only
0AH							MODE		R/W
0BH	SOFT_RST						SET/RESET MODE		R/W
07H	TOUT[5:0]								Read only
08H			TOUT[11:6]						Read only
0CH	Chip ID								Read only

* Warning: All undefined bits in the register must write '0', if it is written '1',the function and performance of the chip will be greatly affected , even the chip may be damaged.

14.2 Register Definition

14.2.1 Output Data Register

Registers 00H ~ 06H store the measurement data from each axis magnetic sensor in themeasurement mode. The data stays the same, regardless of reading status through I^{2}C, until the next measurement data replaces them. Each axis has 18 bit data width in 2's complement, i.e., MSB of 01H/03H/05H/06H indicates the sign of each axis. The output data of each channel saturates between -131072 and 131072.

Table 13 Output Data Register

Addr.	7	6	5	4	3	2	1	0
00H	Data Output X LSB Register XOUT[9:2]							
01H	Data Output X MSB Register XOUT[17:10]							
02H	Data Output Y LSB Register YOUT[9:2]							
03H	Data Output Y MSB Register YOUT[17:10]							
04H	Data Output Z LSB Register ZOUT[9:2]							

05H	Data Output Z MSB Register ZOUT[17:10]							
06H			Data Output Z LSB <1:0>		Data Output Y LSB <1:0>		Data Output X LSB <1:0>	

14.2.2 Temperature Data Registers

Registers 07H-08H store temperature sensor output data. 12 bits temperature sensor output is in 2's complement. Temperature sensor gain is factory-calibrated, but its offset has not been compensated, only relative temperature value is accurate. The temperature coefficient is about 14 LSB/ºC.

Table 14 Temperature Sensor Output

Addr.	7	6	5	4	3	2	1	0
07H	TOUT[5:0]							
08H			TOUT[11:6]					

14.2.3 Control Registers

Two 8-bits registers are used to control the device configurations.

Control register 1 is located in address 0BH, it set soft reset(SOFT_RST).

Control register 2 is located in address 0AH. it sets the operational modes (MODE).

The MODE bit can transfer mode of operations in the device, the two modes are Standby (MODE=0b), and Measurement (MODE=1b). The default mode after Power-on-Reset (POR) is standby. Measurement Mode runs for one millisecond, and then automatically enters Standby Mode. But the MODE bit need to be cleared by software.

Table 15 Control Register 1

Addr	7	6	5	4	3	2	1	0
0BH	SOFT_ RST						SET/RESET	

Reg.	Definition	0	1
SOFT_RST	Reset registers to default value	Normal	Reset and Clear

Reg.	Definition	00	01	10	11
SET/RESET	SET/RESET mode	SET/RESE T	SET	NO SET/RESET	Reserve

Soft Reset can be done by changing the register SOFT_RST to set. Soft reset can be invoked at any time of any mode. For example, if soft reset occurs at the middle of Measurement mode reading, VCM1195L immediately switches to standby mode due to MODE bit is reset to "0" in default.

SOFT_RST: "0": Normal "1": Soft reset, restore default value of all registers.

Table 16 Control Register 2

Addr.	7	6	5	4	3	2	1	0
0AH							MODE	
Reg.	Definition		0		1			
Mode	Mode Control		Standby		Measurement			

14.2.4 Chip ID Register

This register is chip identification register. It returns 0x82.

Table 17 Chip ID Register

Addr.	7	6	5	4	3	2	1	0
0CH	1	0	0	0	0	0	1	0

Ordering Information

Ordering Number	Temperature Range	Package	Packaging
VCM1195L-TR	-40℃~85℃	LGA-16	Tape and Reel: 3k pieces/reel