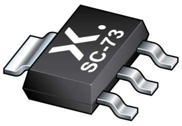


BUK9880-55A

N-channel TrenchMOS logic level FET

19 March 2014 **Product data sheet**

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources

3. Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

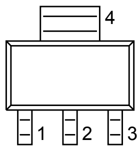
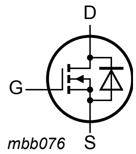
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C		-	-	55	V
I_D	drain current	$V_{GS} = 5$ V; $T_{sp} = 25$ °C; Fig. 3; Fig. 2		-	-	7	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; Fig. 1		-	-	8	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 8$ A; $T_j = 25$ °C		-	62	73	mΩ
		$V_{GS} = 4.5$ V; $I_D = 8$ A; $T_j = 25$ °C		-	-	89	mΩ
		$V_{GS} = 5$ V; $I_D = 8$ A; $T_j = 25$ °C; Fig. 13; Fig. 14		-	68	80	mΩ
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 6$ A; $V_{sup} \leq 55$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped		-	-	36	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SC-73 (SOT223)	
2	D	drain		
3	S	source		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9880-55A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223
BUK9880-55A/CU	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9880-55A	988055A
BUK9880-55A/CU	988055

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C		-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ		-	55	V
V_{GS}	gate-source voltage			-15	15	V
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; Fig. 1		-	8	W
I_D	drain current	$T_{sp} = 100$ °C; $V_{GS} = 5$ V; Fig. 2		-	4	A
		$T_{sp} = 25$ °C; $V_{GS} = 5$ V; Fig. 3; Fig. 2		-	7	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ µs; Fig. 3		-	30	A

Symbol	Parameter	Conditions		Min	Max	Unit
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
V_{GSM}	peak gate-source voltage	pulsed; $t_p \leq 50$ µs		-15	15	V
Source-drain diode						
I_S	source current	T_{sp} = 25 °C		-	7	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{sp} = 25 °C		-	30	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 6 A; $V_{sup} \leq 55$ V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped		-	36	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	Fig. 4	[1][2][3][4]	-	-	J

[1] Maximum value not quoted. Repetitive rating defined in avalanche rating figure.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.
[3] Repetitive avalanche rating limited by an average junction temperature of 145 °C.
[4] Refer to application note AN10273 for further information.

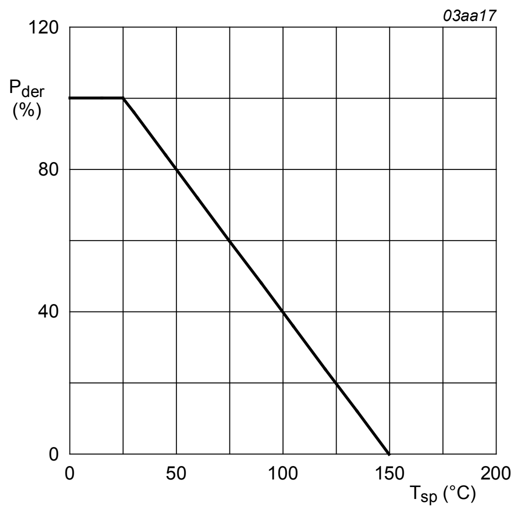


Fig. 1. Normalized total power dissipation as a function of solder point temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

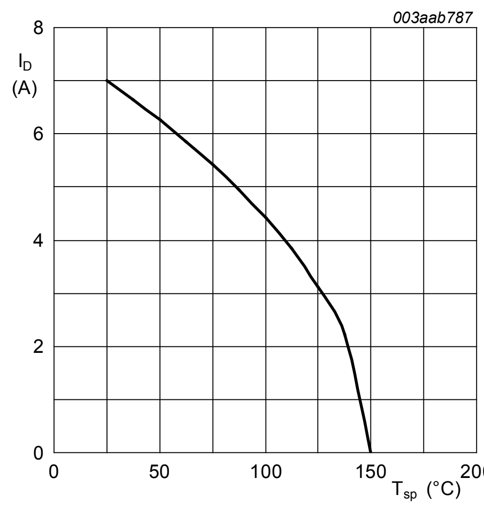


Fig. 2. Continuous drain current as a function of solder point temperature

$$V_{GS} \geq 5\,V$$

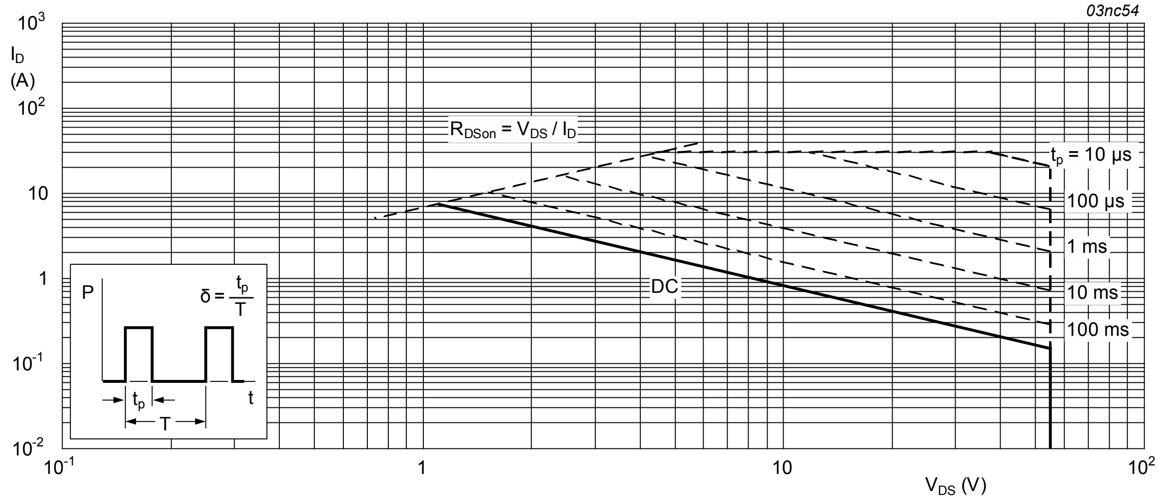


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{amb} = 25°C; I_{DM}$ is single pulse

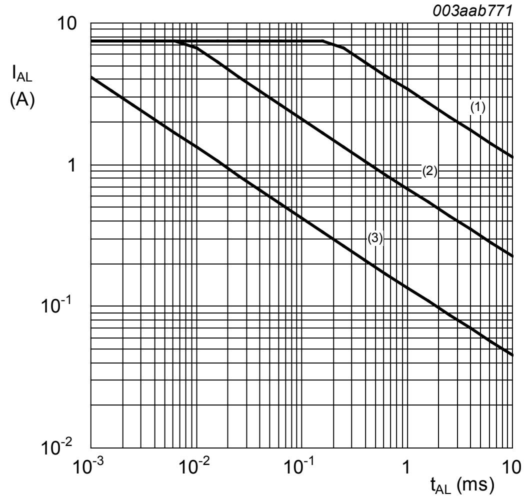


Fig. 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time.

(1) Single-pulse; $T_j = 25$ °C.

(2) Single-pulse; $T_j = 125$ °C.

(3) Repetitive.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	15	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5		-	120	-	K/W

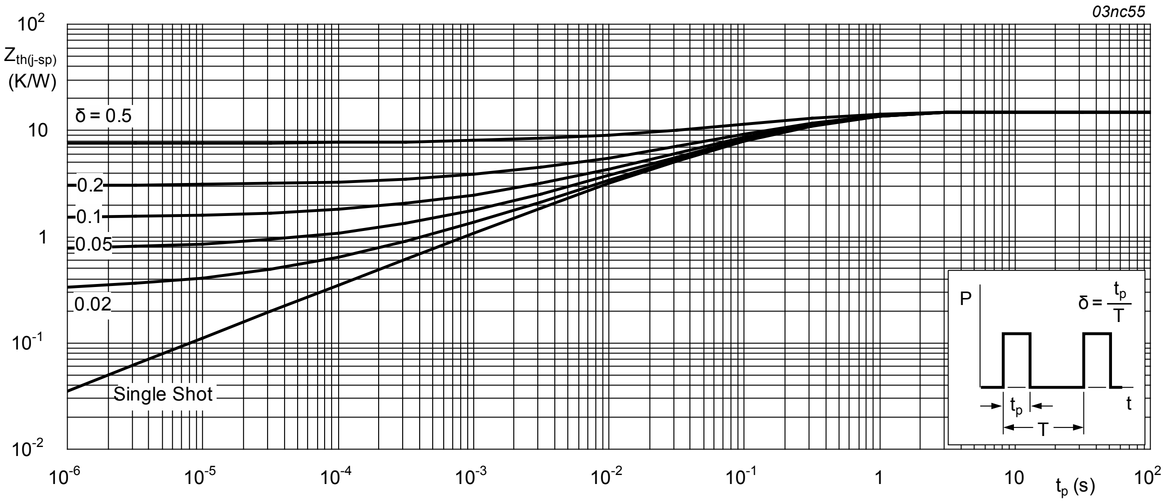


Fig. 5. Transient thermal impedance from junction to solder point as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C		50	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C		55	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 12; Fig. 8		1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; Fig. 12; Fig. 8		0.6	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 12; Fig. 8		-	-	2.3	V
I_{DSS}	drain leakage current	V_{DS} = 55 V; V_{GS} = 0 V; T_j = 150 °C		-	-	500	µA
		V_{DS} = 55 V; V_{GS} = 0 V; T_j = 25 °C		-	0.05	10	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 8 A; T_j = 150 °C; Fig. 13; Fig. 14		-	-	147	mΩ
		V_{GS} = 10 V; I_D = 8 A; T_j = 25 °C		-	62	73	mΩ
		V_{GS} = 4.5 V; I_D = 8 A; T_j = 25 °C		-	-	89	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		V_{GS} = 5 V; I_D = 8 A; T_j = 25 °C; Fig. 13; Fig. 14		-	68	80	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 44 V; V_{GS} = 5 V; Fig. 11		-	11	-	nC
Q_{GS}	gate-source charge			-	1.6	-	nC
Q_{GD}	gate-drain charge	I_D = 10 A; V_{DS} = 44 V; V_{GS} = 5 V; Fig. 15		-	4.6	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	438	584	pF
C_{oss}	output capacitance			-	87	104	pF
C_{rss}	reverse transfer capacitance			-	62	85	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C		-	8	-	ns
t_r	rise time			-	118	-	ns
$t_{d(off)}$	turn-off delay time			-	20	-	ns
t_f	fall time			-	32	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C		-	33	-	ns
Q_r	recovered charge			-	60	-	nC

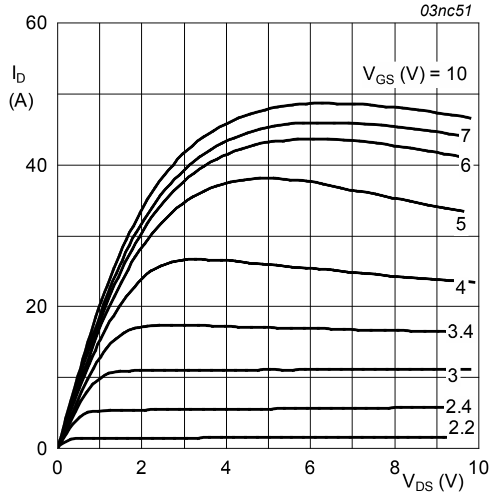


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

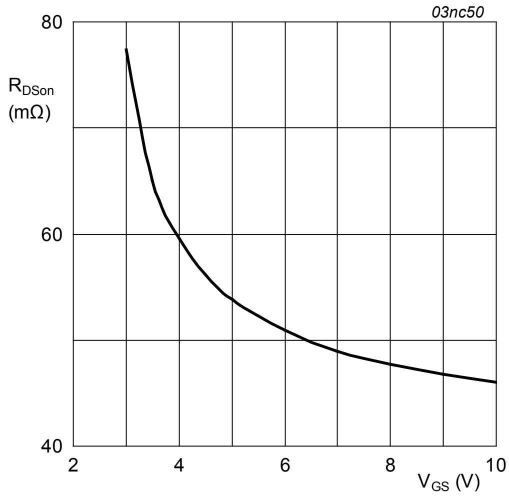
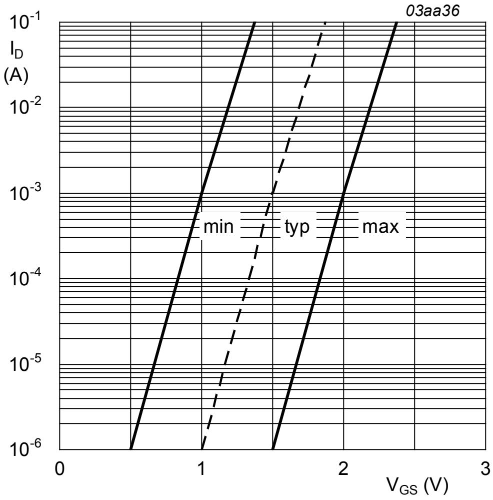


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C; I_D = 10A$



T_j = 25 °C; V_{DS} = 5 V

Fig. 8. Sub-threshold drain current as a function of gate-source voltage

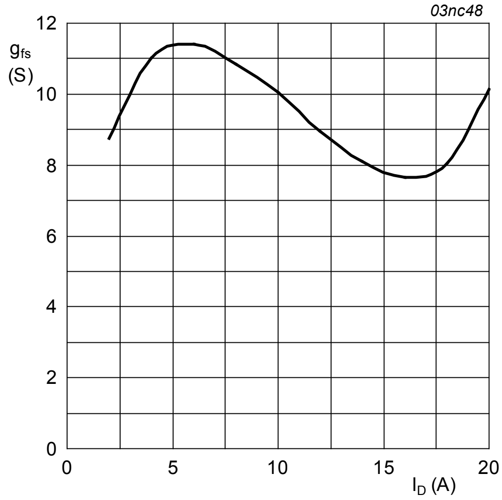


Fig. 9. Forward transconductance as a function of drain current; typical values

$T_j = 25°C; V_{DS} = 25V$

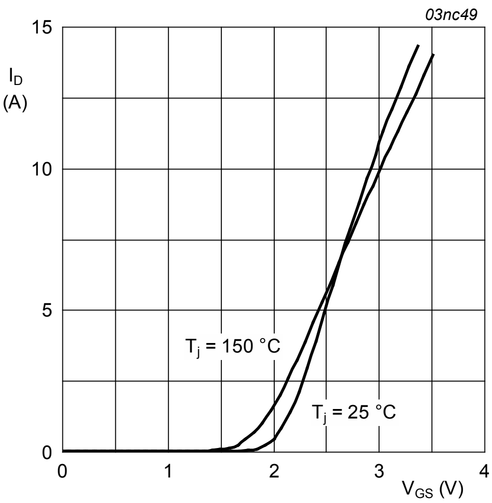


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 25V$

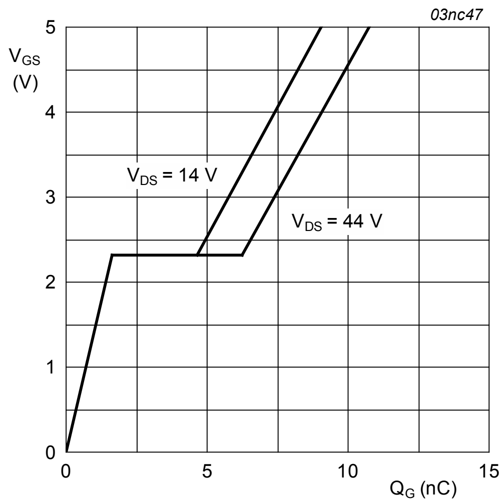


Fig. 11. Gate-source voltage as a function of turn-on gate charge; typical values

$T_j = 25°C; I_D = 10A$

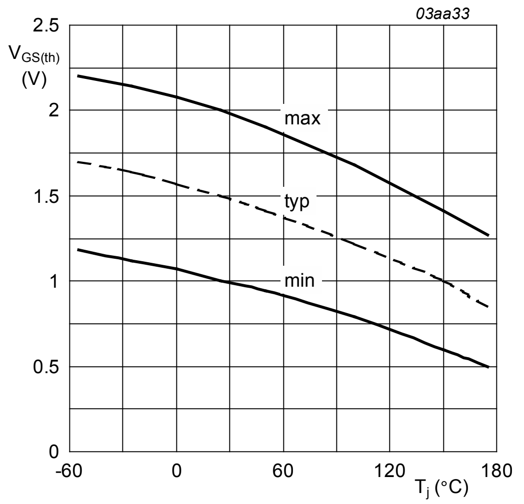


Fig. 12. Gate-source threshold voltage as a function of junction temperature

$I_D = 1mA; V_{DS} = V_{GS}$

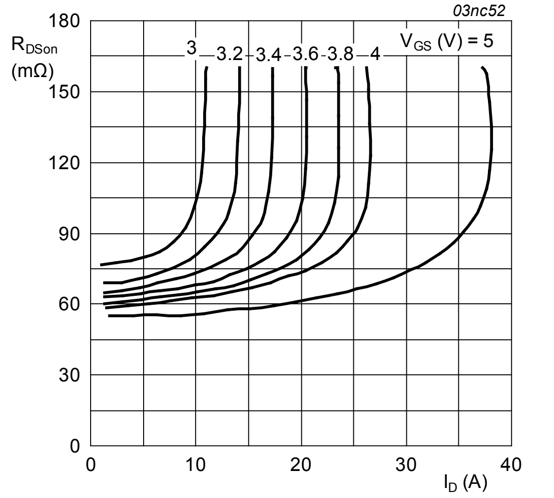


Fig. 13. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

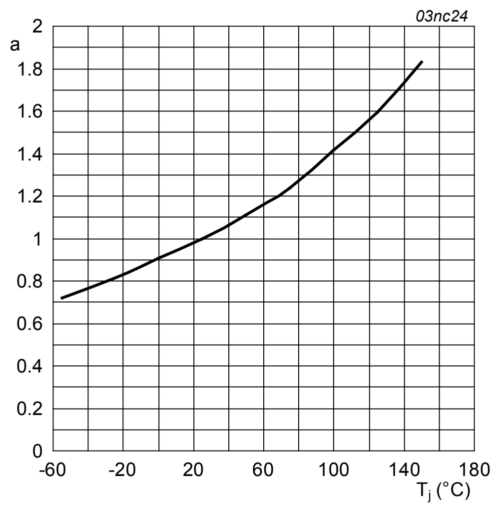


Fig. 14. Normalized drain source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

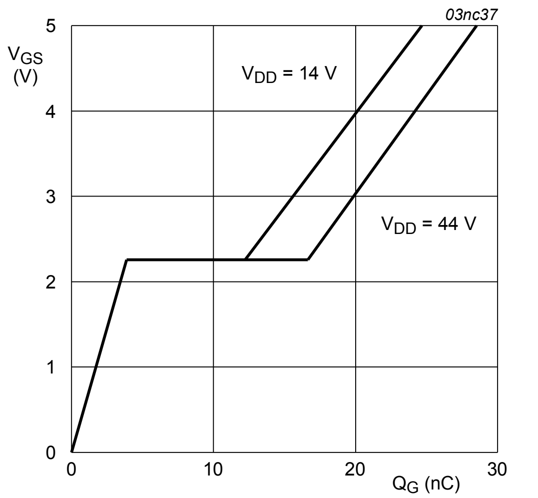


Fig. 15. Gate-source voltage as a function of turn-on gate charge; typical values

$T_j = 25°C; I_D = 15A$

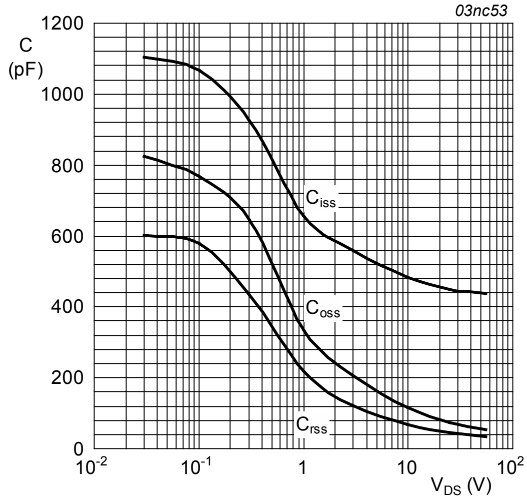


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

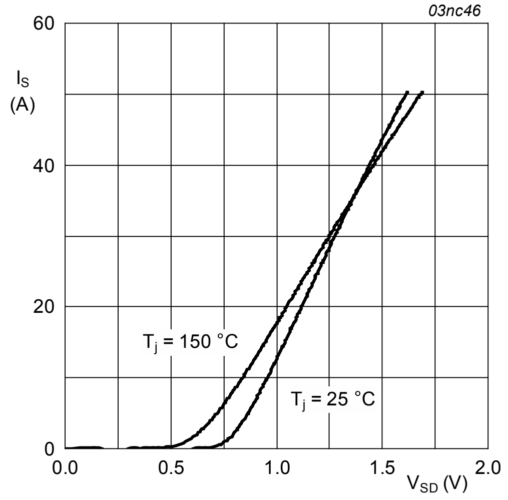
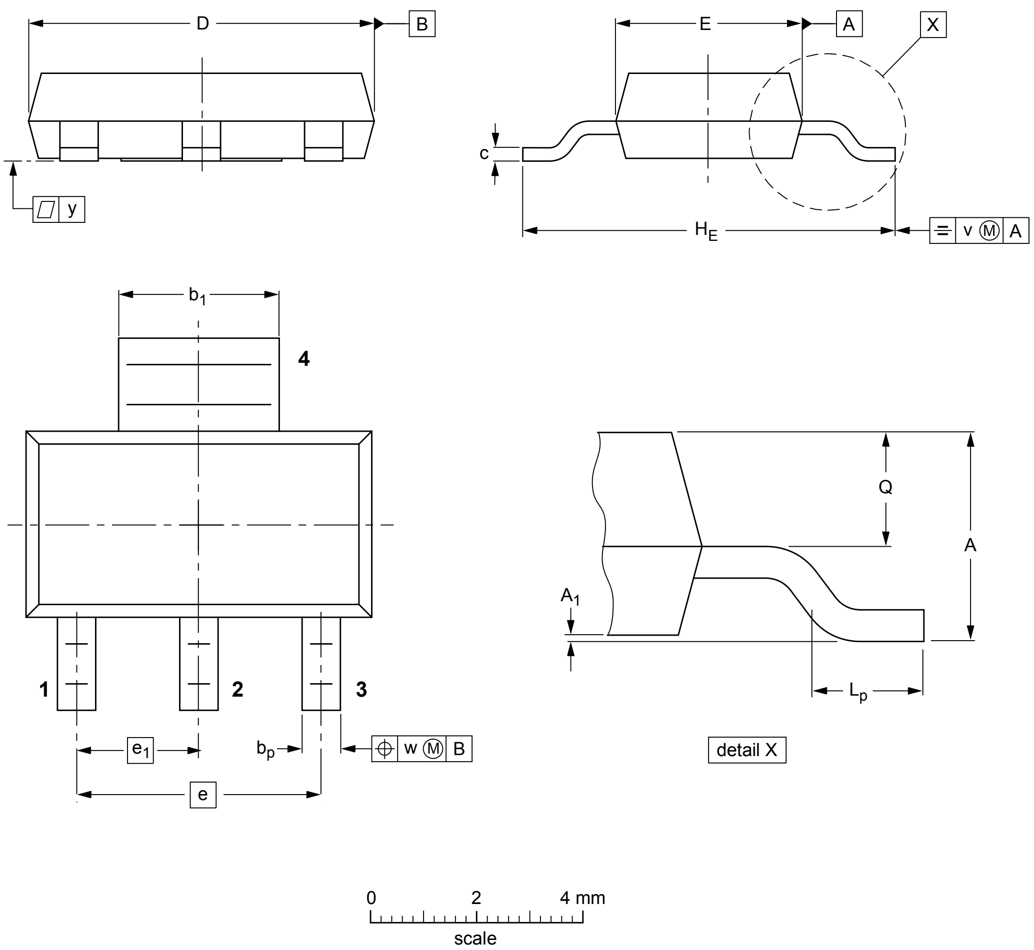


Fig. 17. Reverse diode current as a function of reverse diode voltage; typical value

$V_{GS} = 0V$

11. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

Fig. 18. Package outline SC-73 (SOT223)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

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Date of release: 19 March 2014